



Dolphin PXIe System Switch Module MXP924



MXP924 Users Guide
Version 3.0

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PCI Express External Cabling specification 4.0 is, as of the release of MXP924, not completed and ratified by the PCI-SIG. The MXP924 is designed to the new specification, but Dolphin cannot guarantee the card will be compliant to the final 3.0 version. Dolphin firmware tools can update the CMI implementation.

LIFE SUPPORT POLICY

DOLPHIN INTERCONNECT SOLUTIONS' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES.

ENVIRONMENTAL POLICY

Dolphin is minimizing the amount of printed documentation and software CDs in its shipments; please download additional documentation and software from www.dolphinics.com.

Scope

This version of the MXP924 Users Guide is valid for BMC firmware version 2.4 and newer.

Terms and Acronyms

Important terms and acronyms used in this manual

AOC	Active Optical Cable. PCIe fiber cable assembly available from Dolphin. SFF-8644 connector.
CMI	Cable Management Interface. The 2-wire management interface for communication between subsystems connected by a PCIe 4.0 cable. Details can be found in the PCI-SIG External Cabling Specification 4.0.
BMC	Board Management Controller - Microcontroller on the MXP924 used to manage and implement CMI communications.
eXpressWare	Dolphin's software stack for PCIe clustering and IO. Please visit https://www.dolphinics.com/software for more information.
Lane	One PCI Express Lane contains a differential pair for transmission and a differential pair for reception.
Link	A collection of one or more PCI Express Lanes providing the communication path between an Upstream and Downstream Port.
PCIe 4.0 cable	Cable compliant to the PCI-SIG External Cabling Specification 4.0. Support for CMI. SFF-8644 connector.
Port	PCIe Cable port. The MXP924 has four x4 ports, named P1, P2, P3, P4. These ports can be merged to two x8 ports, or one x16 port. The physical ports are identified by text on the PCIe brackets.
Wake	A mechanism used by a downstream device to request the reapplication of PC main power when in the L2 Link state / Power mode.

MXP924 High Level Specification

The MXP924 is PXIe system switch module and supports a PCIe uplink to a standard PC for PXIe software control. The PC must use a compliant MXH932 card. Up to two MXP924 can be connected to a single MXH932. The MXP924 also supports daisy chaining PXIe Chassis. The MXP924 supports PCIe Gen1, Gen2, Gen3 and Gen4 speeds and x1, x2, x4, x8 and x16 link-widths. The module will operate at the highest common speed shared between the slot and the card (Gen4) and the widest common link-width (x16).

- PCI Express Base Specification, Rev. 4.0
- PCI Express External Cabling specification 4.0
- PCI Express Gen4 16.0 GT/s per lane signaling – 256 GT/s total signaling.
- PCI Express Gen4 x16 edge connector.
- Compliant with PCI Express Gen1 through Gen4 computers and IO systems, auto detection
- The MXP924 supports transparent connections to IO systems (Host and Target operation)
- Quad SFF-8644 cable connector
 - Durability max total 250 mating cycles
- Microchip Switchtec PM40052 PFX PCI Express Gen4 chipset
- 120 nanosecond cut-through latency port to port.
- Support for PCIe Wake functionality.
- Automatic Thermal Shutdown to avoid hardware damages (can be disabled)
- Support for PCIe 4.0 SFF-8644 copper cables.
- Support for SFF-8644 based active optical PCIe complaint fibers (AOC)
- Single System Slot 3U PXI Express, compliant to PXI -5 PXI Express Hardware Specification rev 1.1
- SRNS clocking, Prepared for SRIS clocking
- VAUX powered board management controllers for flexible configuration and cable management
- Flash recovery option. PFX Multi configuration support
- Relative Humidity: 5% - 95% (non- condensing)
- CE and FCC markings

Packaging

The MXP924 product is delivered in a retail box including the following components.

- MXP924 module
- Anti-static bag
- Getting started guide

PXIe System Switch Slot

The MXP924 must be placed in the PXIe system switch slot. The MXP924 supports PCIe Gen1, Gen2, Gen3 and Gen4 speeds. The default PXIe backplane configuration is x16 + x8. The alternative backplane configuration x4 + x4 +x4 +x4 can be enabled by altering the DIP-Switch. The module will auto configure the slot speed and width to match the connected equipment.

MXP924 Configuration

The MXP924 cable ports can either be configured as a single x4 / x8 / x16 PCIe target for connecting to a MXH932 configured for host operation or in daisy-CHANIN mode for connecting x4 / x8 to the host and a single x4 / x8 to a downstream MXP924.

The default DIP switch setting is transparent target x4 / x8 / x16 operations.

Thermal Shutdown

The MXP924 module includes overtemperature overheat protection. The BMC will automatically shut down the MXP924 if a PCIe switch temperature beyond 105°C (221°F) is detected. Similarly, if an AOC is plugged in, the MXP924 module will automatically shut down if the max operating temperature announced by the connected AOC is reached. Please consult the AOC data sheet for details.

NOTE: The MXP924 link LEDs will start flashing yellow when a PCIe switch temperature of 95°C (203°F) is reached or when the AOC reports a temperature 5°C (41°F) lower than the max operating temperature.

NOTE: The automatic shutdown can be disabled by setting DIP switch SW2-4. Prior to disabling the automatic shutdown, please ensure you have established proper airflow.

PCIe Wake

The MXP924 supports PCIe Wake functionality. To utilize this functionality, you need to set the PXH924 DIP-SW2-2 / Enable Wake to ON position and use PCIe 4.0 cables to connect to the MXH932. PCIe Wake must also be enabled in the System BIOS.

Airflow - Operating Environment

To maximize lifetime for the product and maintain the warranty, please honor the specified operating temperature, and make sure the specified air flow is present.

TIP: After installing the Dolphin eXpressWare board management software, you can use the tool `dis_diag` to determine the actual board temperatures.

Cable Connections

The MXP924 is designed to support both long and short PCIe copper cables as well as PCIe active optical cables (AOC).

The MXP924 cable ports are compliant to the SFF-8644 industry specification and supports PCIe cables compliant to the PCIe External Cabling Specification 4.0. Four x4 cables are needed for full PCIe x16 connectivity.

PCI Express 4.0 Cables

When used with cables compliant to the new PCIe External Cable standard 4.0, the MXP924 module will transmit a CMI Reset message downstream. The module can be connected to a MXP924 in Target mode or any PCIe device compliant to the new cable standard.

CMI Functionality

The MXP924 BMC firmware release 2.4 and newer supports the following CMI operations when used with PCIe 4.0 cables:

- Publishes card and CMI status information in readable memory map
- Supports sending and receiving CMI reset, wake and power status messages
- Supports receiving indicators (LED/messages).

Active Optical PCIe Cables (AOC)

Dolphin offers active optical PCIe fiber cables up to 100 meters for the MXP924 module. PCIe AOC cables do not support CWAKE and CPOWERON functionality.

Installation

Step 1 - Unpack board

The MXP924 module is shipped in an anti-static bag to prevent static electricity damage. The module should only be removed from the bag after ensuring that anti-static precautions are taken. Static electricity from your clothes or work environment can damage your MXH924 module or your PXIe components. Always wear a grounded anti-static wrist strap while the MXP924 is removed from the anti-static bag until it is properly installed in the PXIe chassis. Unpack the MXP924 from the anti-static bag using proper anti-static procedures.



Step 2 - Configure the Board for Proper Operation

Set the DIP switch to enable the desired functionality and configuration. Please refer to the section Configuration and DIP Switches on page 10 for details.

Step 3 - Ensure proper Airflow

Please pay proper attention to ensure the selected chassis provides the minimum required airflow.

TIP: Immediately after software installation, please use the dis_diag tool to verify the temperature. If the chip temperature reported by dis_diag exceeds 95°C, it is strongly recommended to improve the airflow.

Step 4 - Install the MXP924

Before installing the module, make sure you are properly grounded to avoid static discharges that may destroy your computer or the PXIe module. Ensure you are properly grounded before opening your PXIe chassis or the anti-static bag containing the MXP924. Please follow your PXIe chassis manual on how to install a PXIe System switch module.



The MXP924 supports PCI Express Gen1, Gen2, Gen3 and Gen4 backplanes. Please review the list of supported and approved PXIe chassis

Step 5 - Installing and Removing the Cable

Installing and removing cables should be done with the PXIe chassis powered off.

Connecting the Cable

Please carefully install the cable connector into the connector housing on the MXP924 module. Cable port 1 is located at the top of the face plate bracket. To install the cable, match the cable house with the connector on the MXP924. Use even pressure to insert the connector until it is secure. Adhere to ESD guidelines when installing the cables to ensure you don't damage the board. Computer cables should always use strain relief to protect the connected equipment from excessive force on the cable. This is especially important for cables between racks.

Cable strain relief

Strain-relief on the PCIe cables are important to protect the PCIe card from fatigue loading and damages. The cable should be mechanically connected to the rack or cabinet. This is especially important for long heavy cables and cables going between cabinets and racks.

Supported cable lengths

The MXP924 supports both copper and active optical PCIe cables (AOC). Maximum lengths between two MXP924 modules can be found in Table 1 below. The maximum distance may change when connecting to other PCIe products.

Cable	Dolphin SKU	Speed	Max Distance
PCIe 4.0 copper cables	PCIe4L-xM	PCIe 4.0	5 meters
PCIe Active Optical cables (AOC)	MSF4C-xM	PCIe 4.0	100 meters
PCIe Active Optical cables (AOC) Pigtail + Patch cable	MSP4M-1M + MTFCCF-xM	PCIe 4.0	102 meters

Table 1: Cable Specifications

Disconnecting the Cable

Please carefully pull the release tab to release the cable from the locking latches and gently pull the cable out of the connector guides.

Step 7 - Verify Installation & LEDs

The MXP924 comes with 4 RGB LEDs which show the corresponding cable port status according to Table 2: LED below. The LEDs are visible through cut-outs in the front panel below each port.

LED color	Function
Off	No cable installed, or PXIe not powered
Yellow	Cable installed, no link
Yellow blinking	Temperature overheat warning, please immediately improve cooling to avoid thermal damage or system shutdown.
White	Cable installed, link operational Gen1 speed
Blue	Cable installed, link operational Gen2 speed
Green blinking	Cable installed, link operational Gen3 speed
Green	Cable installed, link operational Gen4 speed
Red blink	Link Reset

Table 2: LED behavior

Operation

Configuration and DIP Switches

The MXP924 has two banks of 8 DIP switches. The default factory setting for the MXP924 is Transparent Target mode, single (up to x16) link connection.

The MXP924 has DIP switches for setting special modes or operations, the meaning of each DIP switch depends on the loaded firmware. Please carefully read the documentation shipped with the module before modifying any DIP switch settings. Please pay close attention to ON and OFF positions written on the DIP switch.

DIP Switches

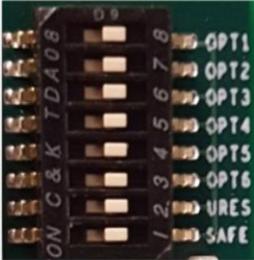


Figure 1: DIP Switch shows the DIP switch for the MXP924. It is used to configure the PCIe module. Please leave all undocumented DIP switches in the default position. Table 3: DIP SW1 settings and Table 4: DIP-SW2 settings below shows all the various DIP switch settings for the MXP924.

Note: DIP switch configuration options may be changed in the future versions. Please always consult the latest user guide for details. The table above is valid for version 1.5.

Figure 1: DIP Switch

DIP-Switch SW1 settings

SW1 DIP no.	Description	ON	OFF	Default
1-8	Configuration selector, details below			OFF

Table 3: DIP SW1 settings

DIP-Switch SW2 settings

SW2 DIP no.	Description	ON	OFF	Default
1	Reserved, leave in Default OFF			OFF
2	Enable Wake	Enable PCIe WAKE	PCIe Wake Disabled	OFF
3	Reserved, leave in Default OFF			OFF
4	Disable thermal shutdown	Thermal shutdown disabled	Shut down the switch if critical temperature reached.	OFF
5-8	Reserved, leave in Default OFF			OFF

Table 4: DIP-SW2 settings

DIP switch Settings

The following DIP Switch settings should be considered when configuring the **MXP924**:

DIP Switch settings for MXP924 operation – DIP-Switch-1

The following DIP-1 Switch settings should be considered when configuring the **MXP924**:

Config	Use Case	Configuration MXP924	DIP SW1	DIP switch view
0	A+B	<ul style="list-style-type: none"> Single Transparent Target One x4 / x8 / x16 upstream port (P1+P2+P3+P4) x16 + x8 Backplane Hot Plug Enabled 	<p>(all off)</p> <p>(Shipping Default)</p>	
1	B+C	<ul style="list-style-type: none"> Transparent Target / Daisy chain One x4 / x8 upstream port (P1+P2) One x4 / x8 downstream port (P3+P4) x16 + x8 Backplane Hot Plug Enabled 	1: ON	
2	A+B	<ul style="list-style-type: none"> Single Transparent Target One x4 / x8 / x16 upstream port (P1+P2+P3+P4) x4 + x4 + x4 + x4 Backplane Hot Plug Enabled 	2: ON	
3	B+C	<ul style="list-style-type: none"> Transparent Target / Daisy chain One x4 / x8 upstream port (P1+P2) One x4 / x8 downstream port (P3+P4) x4 + x4 + x4 + x4 Backplane Hot Plug Enabled 	<p>1:ON</p> <p>2:ON</p>	
8	A+B	<ul style="list-style-type: none"> Single Transparent Target One x4 / x8 / x16 upstream port (P1+P2+P3+P4) x16 + x8 Backplane Hot Plug Disabled 	4:ON	
9	B+C	<ul style="list-style-type: none"> Transparent Target / Daisy chain One x4 / x8 upstream port (P1+P2) One x4 / x8 downstream port (P3+P4) x16 + x8 Backplane Hot Plug Disabled 	<p>1:ON</p> <p>4:ON</p>	
10	A+B	<ul style="list-style-type: none"> Single Transparent Target One x4 / x8 / x16 upstream port (P1+P2+P3+P4) x4 + x4 + x4 + x4 Backplane Hot Plug Disabled 	<p>2:ON</p> <p>4:ON</p>	
11	B+C	<ul style="list-style-type: none"> Transparent Target / Daisy chain One x4 / x8 upstream port (P1+P2) One x4 / x8 downstream port (P3+P4) x4 + x4 + x4 + x4 Backplane Hot Plug Disabled 	<p>1:ON</p> <p>2:ON</p> <p>4:ON</p>	

Use Cases

The MXP924 module may be used to connect the PXIe chassis to a PC utilizing a MXH932. A PC can connect to several MXP924 using a single or multiple MXH932. The MXH924 can also be used to daisy chain PXIe chassis. The supported use cases and the DIP switch settings are summarized in section Configuration and DIP Switches on page 10. DIP-Switch settings for the MXH932 card can be found in the MXH932 Users Guide available from www.dolphinics.com.

Use Case A - 1 Host – Single PXIe Configuration - PCIe x16

The Host system has a MXH932 adapter configured for Host operation and a direct x4, x8 or x16 link to a MXP924. If you are not using all four ports, please always start connecting the lower port numbers.

The MXP924 DIP-1 Switch should be set to Config 0: Single Target config.

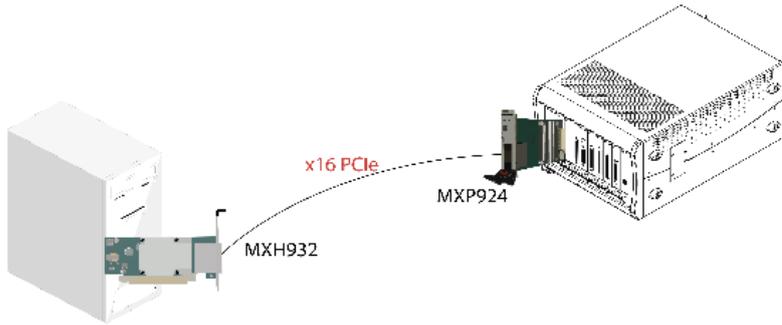


Figure 2: Use Case A

MXH932 Host card ports	MXP924 ports
P1	P1
P2	P2
P3	P3
P4	P4

Table 5: Required x16 cabling

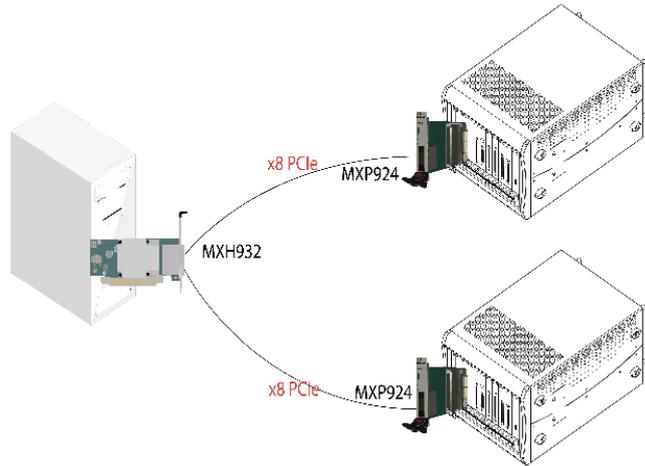
Always connect a cable from Port #x to Port #x

A failure connecting any of the cables will cause the link to re-train to x8 or x4.

Use Case B – 1 Host – Single or Dual PXle Configuration – PCIe x8

The host has an MXH932 adapter configured for Transparent Host operation and a direct x8 link is used to connect one or two PXle systems utilizing a MXP924's. Please note, always use MXP924 port P1 and P2 on both systems. If you are only connecting a single x4 cable, please only use port P1 on both systems.

The MXP924 DIP-1 Switch should be Config 0: Single Target config or Config 1: Transparent Target / Daisy chain.



MXH932 Host card ports	MXP924 Target 1 ports	MXP924 Target 2 ports
P1	P1	
P2	P2	
P3		P1
P4		P2

Table 6: Required x8 cabling

Use Case C – 1 Host – Daisy chain PXIe Configuration – PCIe x8

The host has an MXH932 adapter configured for Transparent Host operation. Two or more MXP924 switches are connected in a daisy chain. Port P1 and P2 are upstream. Port P3 and P4 are downstream.

The MXP924 DIP-1 Switch should be Config 1: Transparent Target / Daisy chain.

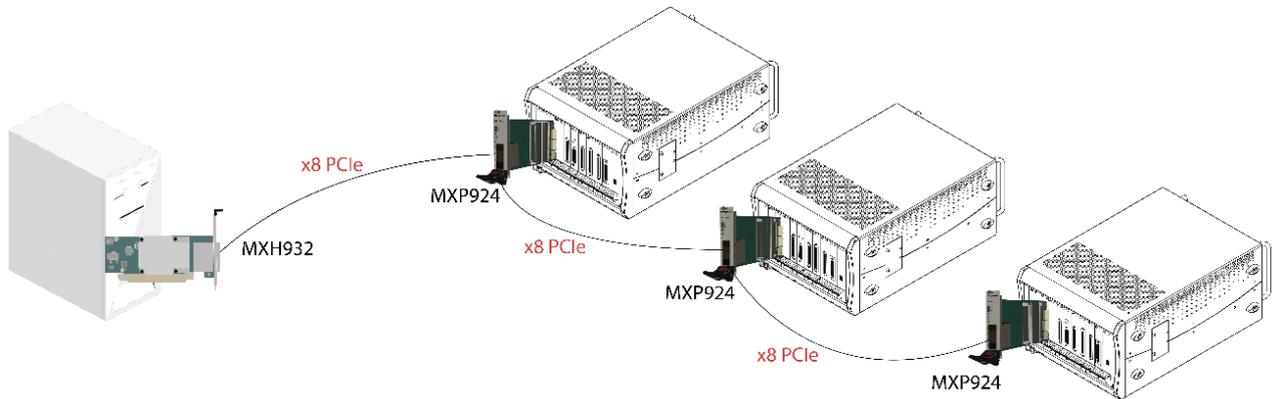


Figure 3: Use Case C

MXH932 Host card ports	MXP924 Target card 1 port	MXP924 Target card 2 ports	MXP924 Target card 2 ports
P1	P1	P3	P1
P2	P2	P4	P2
	P3	P1	
	P4	P2	

Table 7: Required x4 cabling

EEPROM and Firmware Upgrade

The MXP924 design uses a Board Management Controller (BMC) to implement the PCIe CMI protocol, reset and other maintenance functions. Dolphin may from time to time publish updated firmware for the BMC, PCIe switch or EEPROM data for the card.

WARNING: Please note that standard Microsemi tools (ChipLink) cannot be used to upgrade the firmware as this will violate the warranty. Please contact Dolphin for instructions on how to upgrade the MXP924 firmware.

Note: Please consult the MXP924 Firmware Release Note for details on supported configurations.

Identifying the PXIe module

The module has a label-sticker with the serial number in the format 'MXP924-YY-ZZZZZ', where YY denotes the revision (e.g. BB) and ZZZZZ denotes the serialized production number (e.g. 012345) – this whole string makes up the serial number of the module (i.e. MXP924-CC-012345).

You can also get this information using `lspci` in Linux:

First, identify the devices for the Dolphin Host card:

```
# lspci | grep "Device 4052"
01:00.0 PCI bridge: PMC-Sierra Inc. Device 4052
01:00.1 Bridge: PMC-Sierra Inc. Device 4052
02:00.0 PCI bridge: PMC-Sierra Inc. Device 4052
```

Then run lspci and identify the module. It will show up as something like

```
# lspci -s 1:0.0 -v
01:00.0 PCI bridge: PMC-Sierra Inc. Device 4052 (prog-if 00 [Normal decode])
  Flags: bus master, fast devsel, latency 0, IRQ 122
  Bus: primary=01, secondary=02, subordinate=03, sec-latency=0
  I/O behind bridge: 00002000-00002fff
  Prefetchable memory behind bridge: 00000000c8000000-00000000c81ffff
  Capabilities: [40] Express Upstream Port, MSI 00
  Capabilities: [7c] MSI: Enable+ Count=1/8 Maskable- 64bit+
  Capabilities: [8c] Power Management version 3
  Capabilities: [94] Subsystem: Dolphin Interconnect Solutions AS Device 0924
  Capabilities: [100] Advanced Error Reporting
  Capabilities: [148] Power Budgeting <?>
  Capabilities: [158] #12
  Capabilities: [188] #19
  Capabilities: [1b4] Device Serial Number 00-00-43-43-00-00-00-24
  Capabilities: [1c0] Latency Tolerance Reporting
  Capabilities: [1c8] Access Control Services
  Capabilities: [1f0] #25
  Capabilities: [1fc] #26
  Capabilities: [23c] #27
  Capabilities: [7f8] Vendor Specific Information: ID=ffff Rev=1 Len=808 <?>
  Kernel driver in use: pcieport
  Kernel modules: shpchp
```

Second, do

```
# lspci -s 1:0.0 -v | grep -E "Subsystem|Serial"
  Capabilities: [a4] Subsystem: Dolphin Interconnect Solutions AS Device 0932
  Capabilities: [100] Device Serial Number 00-00-42-42-00-00-00-ff
```

This shows the module as revision 0x4242 (hexadecimal values of the 'BB' letters in the ASCII table), with the production number 0x000000ff (00000255 in decimal).

Support

More information about the product, support and software download can be found at <http://www.dolphinics.com/mx>.

For general support questions, please contact Dolphin via the Jira Service Management portal: <https://www.dolphinics.com/csp>.

Technical Information

Board revision history

The following table gives a general overview of the hardware revision history.

MXP924 revision	Capabilities
MXP924-BB	<ul style="list-style-type: none"> Initial version for testing. Not available
MXP924-CC	<ul style="list-style-type: none"> Production version
MXP924-CD	<ul style="list-style-type: none"> Minor adjustment of LED intensity on port 1 to align with other ports.

PCIe Cable Port Signals

The external PCI Express SFF-8644 cable connector supports the following signals:

- PETpN/PETnN: PCI Express Transmitter pairs, labeled where N is the Lane number (starting with 0); “p” is the true signal while “n” is the complement signal.
- PERpN/PERnN: PCI Express Receiver pairs, labeled where N is the Lane number (starting with 0); “p” is the true signal while “n” is the complement signal.
- PWR: Power to support AOC and signal conditioning components within the cable assembly.
- MGTPWR: Power supplied to the connector for cable management components that are needed while the link is not active. This needs to be active if the subsystem has power.
- CBLPRSNT#: Cable present detect, an active-low signal pulled-down by the cable when it is inserted into the MXP924 connector.
- CADDR: Signal used to configure the upstream cable management device address.
- CINT#: Signal asserted by the cable assembly to indicate a need for service via the CMI controller.
- CMISDA: Management interface data line. Used for both initial link setup and sideband messages when used with CMI compliant cables.
- CMISCL: Management interface clock line. Used for both initial link setup and sideband messages when used with CMI compliant cables.

External PCIe x4 Cable Connector Pin-Out

Row	9	8	7	6	5	4	3	2	1
D	GND	PETn2	PETp2	GND	PETn1	PETp1	GND	MGTPWR	PWR
C	GND	PETn3	PETp3	GND	PETn0	PETp0	GND	CMISDA	CMISCL
B	GND	PERn2	PERp2	GND	PERn1	PERp1	GND	CBLPRSNT#	PWR
A	GND	PERn3	PERp3	GND	PERn0	PERp0	GND	CINT#	CADDR

Table 8; External PCIe x4 cable Pin-Out

PCIe Cable Port Mapping

The MXP924 module has a quad SFF-8644 connector. The table below shows the signal / port map.

Cable Port	x16	Dual x8	Quad x4	PCIe 3.0 Cable Pin
1	L0	L0	L0	TX0/RX0
	L1	L1	L1	TX1/RX1
	L2	L2	L2	TX2/RX2
	L3	L3	L3	TX3/RX3
2	L4	L4	L0	TX0/RX0
	L5	L5	L1	TX1/RX1
	L6	L6	L2	TX2/RX2
	L7	L7	L3	TX3/RX3
3	L8	L0	L0	TX0/RX0
	L9	L1	L1	TX1/RX1
	L10	L2	L2	TX2/RX2
	L11	L3	L3	TX3/RX3
4	L12	L4	L0	TX0/RX0
	L13	L5	L1	TX1/RX1
	L14	L6	L2	TX2/RX2
	L15	L7	L3	TX3/RX3

Lx – PCIe lane X, Cable port is ref PCIe bracket marking

Table 9 : PCIe Cable Port Mapping

Compliance and Regulatory Testing

EMC Compliance

The Dolphin PXIe MXP924 system switch is tested to comply with the following standards:

- EN 61326-1:2013
- EN 61000-6-1 :2007
- KS C IEC 61326-1:2008
- KS C IEC 61000-6-1:2002
- 47 CFR Part 15. Subpart B (Clause 15.107 and 15.109) in conjunction with ANSI C63.4:2014



This does not ensure that it will comply with these standards in any random PXIe chassis. It is the responsibility of the integrator to ensure that their products are compliant with all regulations where their product will be used.

FCC Class A

This equipment is tested to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules.



RoHS Compliance

The Dolphin MXP924 is RoHS compliant. A Compliance certificate issued by the manufacturer is available upon request.



WEEE Notice

The PXIe module is labelled in accordance with European Directive 2002/96/EC concerning waste electrical and electronic equipment (WEEE). The Directive determines the framework for the return and recycling of used appliances as applicable throughout the European Union. This label is applied to products to indicate that the product is not to be thrown away but returned to your local approved WEEE waste collector.



Limited Warranty

Dolphin Interconnect Solutions warrants this product to be free from manufacturing defects under the following terms:

Warranty Period

The warranty applies for one (1) year from the date of purchase. Extended warranty is available.

Coverage

To the extent permitted by applicable law, this warranty does not apply to:

- Damage caused by operator error or non-compliance with instructions available for the product.
- Use or attempt to use or program firmware not approved by Dolphin.
- Damage due to accidents, abuse, misuse, improper handling or installation, moisture, corrosive environments, high voltage surges, shipping, or abnormal working conditions.
- Damage caused by acts of nature, e.g. floods, storms, fire, or earthquakes.
- Damage caused by any power source out of range or not provided with the product.
- Normal wear and tear.
- Attempts to repair, modify, open, or upgrade the product by personnel or agents not authorized by Dolphin.
- Products for which the serial number label has been tampered with or removed.
- Damage to the product caused by products not supplied by Dolphin.

Service Procedure

In the event that the product proves defective during the Warranty Period, you should contact the seller that supplied you with the product, or if you purchased it directly from Dolphin, visit <https://www.dolphinics.com/csp> to obtain a valid RMA number and instructions. Products returned to Dolphin without a proper RMA number will not be serviced under this warranty.