SG1010- A3 Errata

Revision 3

Date: March 2011

Bundled Link Operation

Bundled links are subject to the following limitations:

Link Disable:

The Link Disable bit must not be set for an operational link in a bundle if traffic may be flowing over that link. Either ensure traffic is quiesced, or take the port down by clearing the Traffic Enable bit for one of the links.

Single Link disconnect:

A single link in an operational bundle cannot be disconnected. If a cabling solution is desired, a custom cable that disconnects both links at the same time is required.

Multicast Traffic:

Heavy multicast traffic transmitted out of a bundle may result in data corruption, credit problems, and a chip/system hang. Multicast traffic should not be sent out bundled links.

Fabric Enumeration:

When two links of a SG1010 switch are connected to the same link partner in a bundled configuration, the port may not properly enumerate. When this erratum occurs, only one link partner believes it is part of the bundled port. Any read transaction that traverses the affected link may not properly return data to the initiator of that read. An address routed system with this configuraton will hang during BIOS initialization when this erratum is encountered. A similarly configured path routed only system will hang during fabric discovery. This erratum will never affect a bundled port between a root SG2010 and an SG1010 switch.

Potential workarounds for this erratum include:

1. Don't use bundled ports with the SG1010 for new designs.

2. If hardware has already been fabricated with bundled ports on a SG1010 switch, one of the links in the bundled port(s) can be disabled by setting the appropriate LDIS bit (bit 4 in the Link Control and Status register*). The LDIS bit, which disables a link by turning off its transmitters, needs to be set using the SG1010's SROM interface. The following are the Control and Status register offsets for the six SG1010 links:

   Link 0 – 0x200
   Link 1 – 0x240
   Link 2 – 0x280
   Link 3 – 0x2c0
   Link 4 – 0x300
   Link 5 – 0x340

   * For more details on the SG1010 Link Control and Status register please refer to section 4.6.1.1 of the SG1010 Hardware Reference Manual.

3. If using the StarGen driver, the fabric root can be established using software (i.e. pseudo-

root). The bundling erratum is not seen when fabric enumeration is performed via software.

JTAG

PLL_RESET pin is not a part of the JTAG scan chain.

Silicon Revision ID

The value of the Silicon Revision ID register was not changed between the SG1010-A2 and SG1010-A3 revision changes. Reading the Silicon Revision ID register, located at offset 0x000Ch in the SG1010-A3's StarFabric Component Header registers, returns a value of 0x00000001h. This dword value is the same as the SG1010-A2's Silicon Revision ID.

Use the SG1010's serial ROM interface to preload a unique value such as 0x00000002h in the StarFabric Component Header register called SFC Programming Interface ID, which is located at offset 0x001Ch. This register is initialized to 0x00000000h at reset, but is loadable only through the serial ROM interface. The user can utilize this register to uniquely identify the SG1010-A3 from the SG1010-A2 if it is critical in their application.

Path Invalidate Frame not sent

A path invalidate frame is not sent if a port is down by setting LDIS register bit by software. The lack of a path invalidate frame being sent to the source device results in subsequent frames will get no response from the down port. The source device will receive a tineout event or an unexpected response.

A path invalidate frame will be sent as specified if the port was disabled by disconnecting link signal lines or if an adjacent device port was disabled by software.

Avoid sending frames to intentionally disabled port